## AMENDMENTS TO THE CLAIMS

1. (Original) A semiconductor device comprising:

a semiconductor chip; and

a plurality of electrodes, which are connected with the semiconductor chip and are enclosed in a resin package in such a way that surfaces of the electrodes are exposed to a surface of the resin package,

wherein the surfaces of the electrodes are arranged inwardly of a prescribed area surrounded by a plurality of bonding pads of the semiconductor chip.

2. (Original) A semiconductor device according to claim 1, wherein a plurality of bumps or balls are respectively attached onto the exposed surfaces of the electrodes.

3. (Original) A semiconductor device according to claim 2, wherein the plurality of bumps or balls are each made of solder, gold, silver, copper, or an alloy including at least two elements selected from among gold, silver, and copper, or an conductive polymer.

4. (Original) A semiconductor device according to claim 1, wherein a plurality of cutting grooves are formed on the surface of the resin package, on which the surface of the electrodes are exposed, by half dicing.

5. (Original) A semiconductor device according to claim 1, wherein the plurality of electrodes are supported by a plurality of electrode supports interconnected with a lead frame and embedded in the resin package.

6. (Original) A semiconductor device according to claim 4, wherein the plurality of electrodes are supported by a plurality of electrode supports interconnected with a lead frame and embedded in the resin package.

7. (Original) A semiconductor device according to claim 6, wherein the electrode supports are partially cut out so that cut surfaces thereof are exposed to at least one cutting groove.

8. (Original) A semiconductor device according to claim 6, wherein the electrode supports are partially cut out so that cut surfaces thereof are exposed to both of side walls of at least one cutting groove.

9. (Original) A semiconductor device according to claim 5, wherein the lead frame comprises a plurality of outer frames, each of which includes a plurality of irregularities.

10. (Original) A semiconductor device according to claim 6, wherein the lead frame comprises a plurality of outer frames, each of which includes a plurality of irregularities.

11. (Original) A semiconductor device according to claim 10, wherein at least one outer frame is subjected to cutting so that cut surfaces of the irregularities are exposed to a bottom of at least one cutting groove.

12. (Presently Amended) A semiconductor device according to ~~any one of claims 9 to 11~~ claim 9, wherein the plurality of irregularities comprise a series of projections and hollows, which are continuously and alternately arranged along the outer frame.

13. (Original) A semiconductor device according to claim 9, wherein the lead frame further comprises an intermediate frame for partitioning an area defined by the plurality of outer frames.

14. (Original) A semiconductor device according to claim 10, wherein the lead frame further comprises an intermediate frame for partitioning an area defined by the plurality of outer frames.

15. (Original) A semiconductor device according to claim 9, wherein the plurality of electrode supports are respectively connected with a plurality of hollows within the plurality of irregularities.

16. (Original) A semiconductor device according to claim 10, wherein the plurality of electrode supports are respectively connected with a plurality of hollows within the plurality of irregularities.

17. (Original) A manufacturing method for a semiconductor device comprising the steps of:

pressing a metal material to produce a lead frame that comprises a plurality of outer frames, a plurality of electrode supports connected with the plurality of outer frames, and a plurality of electrodes respectively supported by the plurality of electrode supports;

drawing the plurality of electrode supports to be lowered in position compared with surfaces of the electrodes and at least a part of the outer frames;

forming a lead frame assembly in which a semiconductor chip is electrically connected with the plurality of electrodes;

enclosing the lead frame assembly within a resin package in such a way that the surfaces of the electrodes are exposed to a surface of the resin package; and

cutting at least a prescribed part of the electrode supports so as to separate the plurality of electrodes from each other.

18. (Original) The manufacturing method for a semiconductor device according to claim 17 further comprising the steps of:

effecting metal plating on the exposed surfaces of the electrodes respectively; and forming a plurality of bumps or balls on the plated surfaces of the electrodes.

19. (Original) The manufacturing method for a semiconductor device according to claim 18, wherein after the plurality of bums or balls are formed on the plated surfaces of the electrodes, the prescribed part of the electrode supports are cut out so that the plurality of electrodes are separated from each other.

20. (Original) The manufacturing method for a semiconductor device according to claim 18, wherein the plurality of bumps or balls are each made of solder, gold, silver, copper, or an alloy including at least two elements selected from among gold, silver, and copper, or an conductive polymer.

21. (Original) The manufacturing method for a semiconductor device according to claim 17, wherein the lead frame is subjected to press working so that a plurality of irregularities comprising a series of projections and hollows are formed along at least one outer frame, and wherein each of the projections is positioned at a height substantially matching the surface of each electrode, and each of the hollows is positioned at a height which is lower than the surface of each electrode.

22. (Original) The manufacturing method for a semiconductor device according to claim 17, wherein the lead frame further comprises an intermediate frame substantially positioned at a center of an area defined by the outer frames.

23. (Original) The manufacturing method for a semiconductor device according to claim 17, wherein the plurality of electrode supports are drawn in position in accordance with one of etching, polishing, and press working.

24. (Original) The manufacturing method for a semiconductor device according to claim 21, wherein the electrode supports are subjected to cutting such that summit portions of the projections arranged along the outer frame are cut out.

25. (New) A semiconductor device according to claim 10, wherein the plurality of irregularities comprise a series of projections and hollows, which are continuously and alternately arranged along the outer frame.

26. (New) A semiconductor device according to claim 11, wherein the plurality of irregularities comprise a series of projections and hollows, which are continuously and alternately arranged along the outer frame.